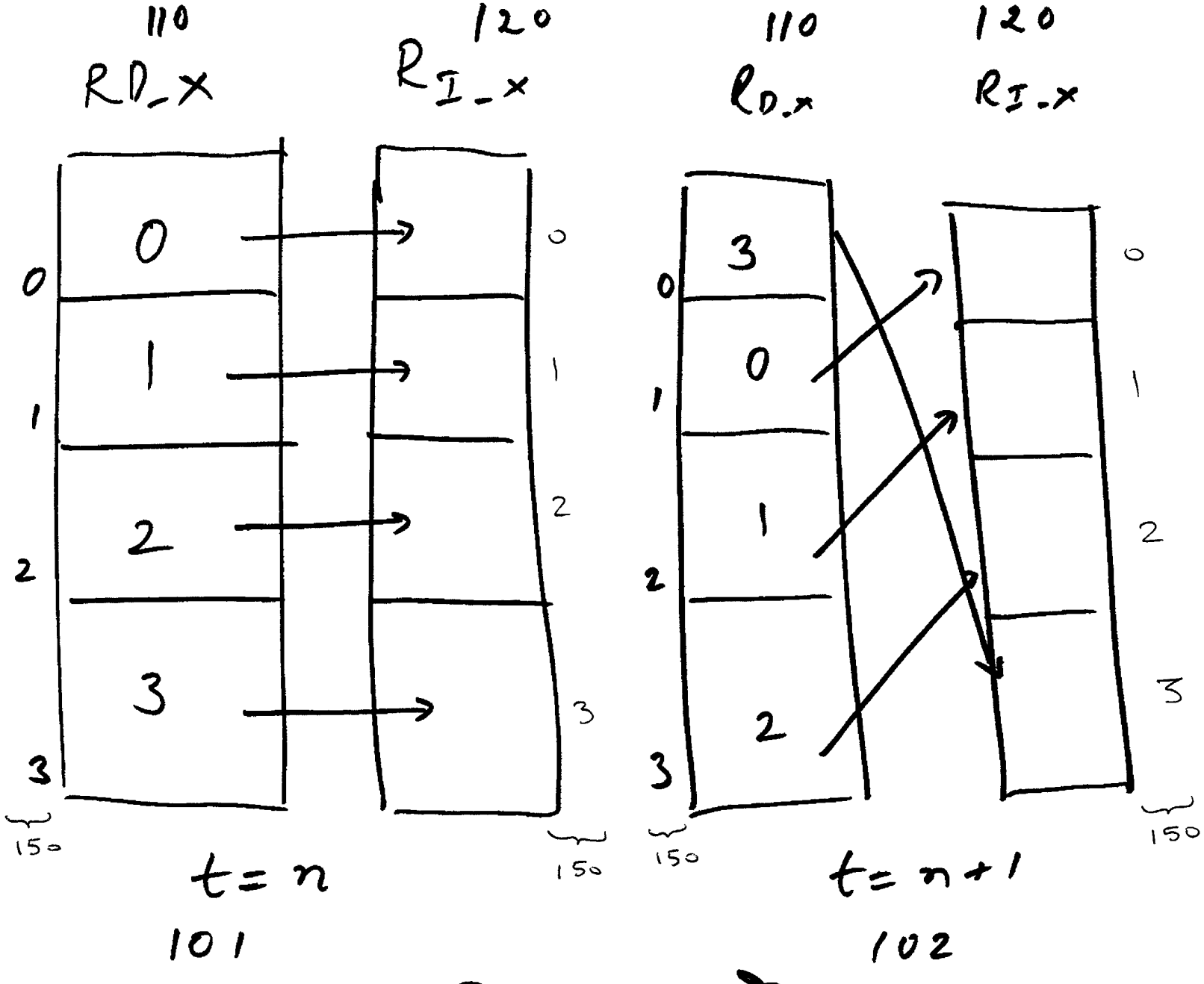


Fig 1.

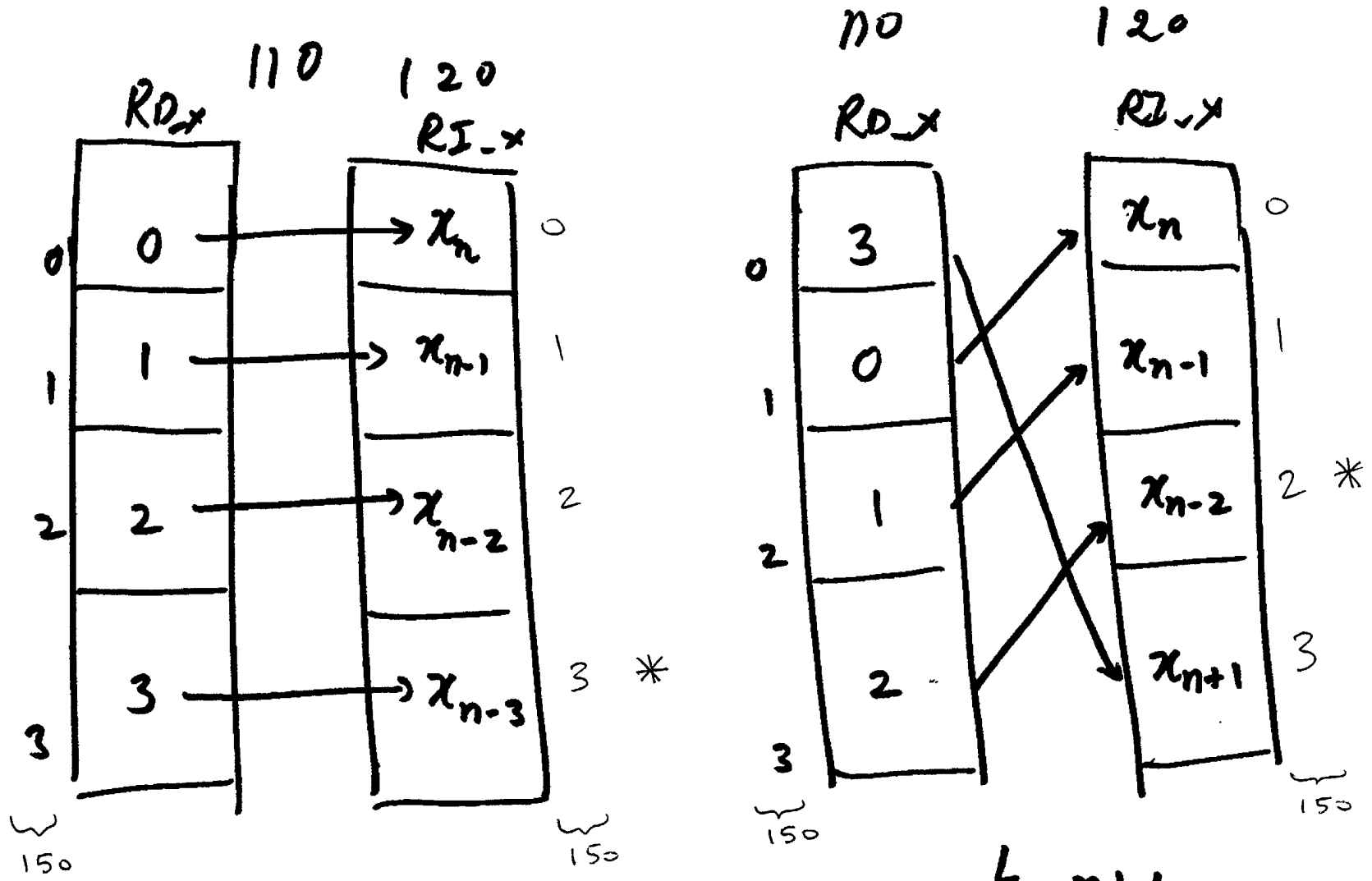
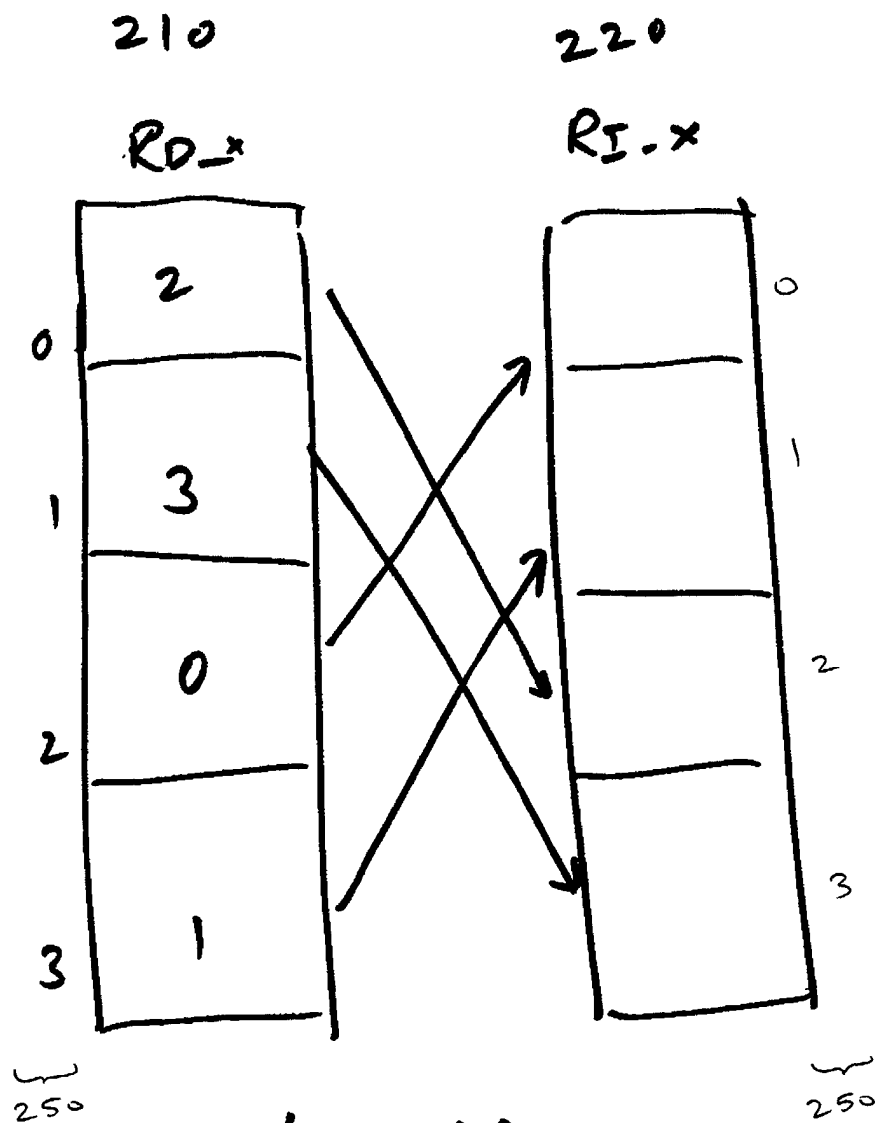

110
120
RD_x
RI_x
0
1
2
3
x_n
x_{n-1}
x_{n-2}
x_{n-3}
*
150
t = n
101
110
120
RD_x
RI_x
3
0
1
2
x_n
x_{n-1}
x_{n-2}
x_{n+1}
*
150
t = n+1
102

Fig. 1A.

Figure 2


210
220
RD_x
RI_x
2
3
0
1
0
1
2
3
0
1
2
3
250
250
t = n+2
201

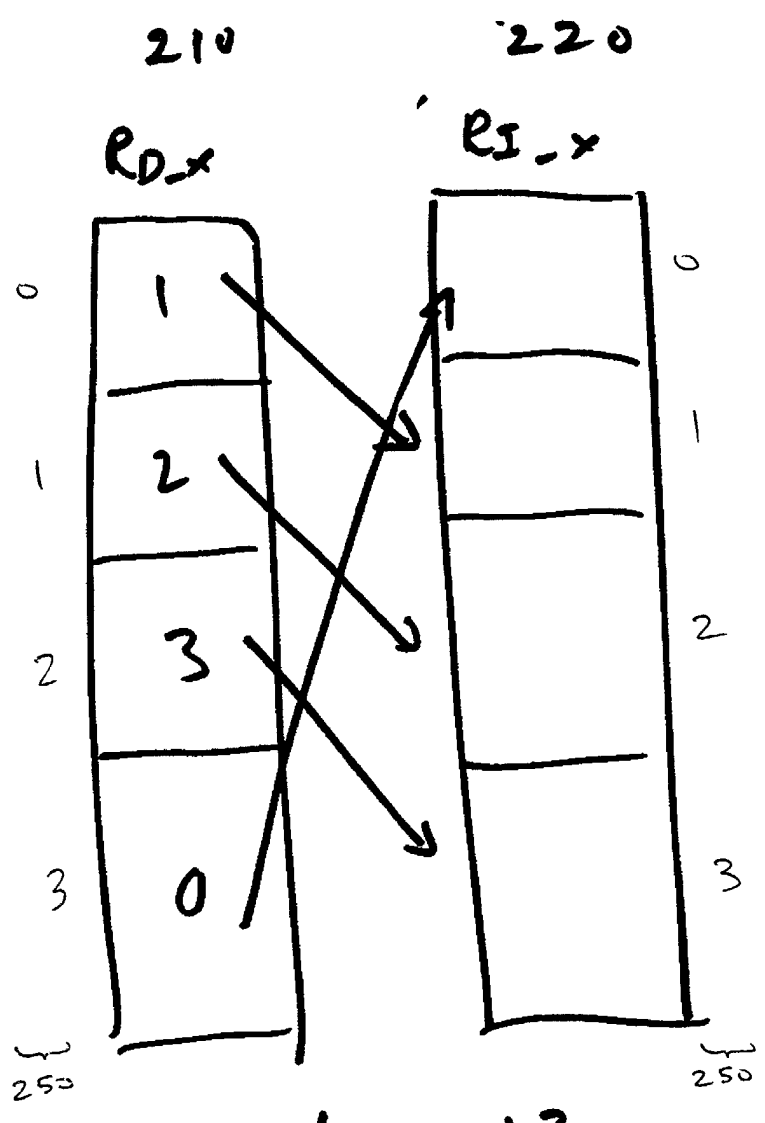

210
220
RD_x
RI_x
1
2
3
0
0
1
2
3
0
1
2
3
250
250
t = n+3
202

FIGURE 2A

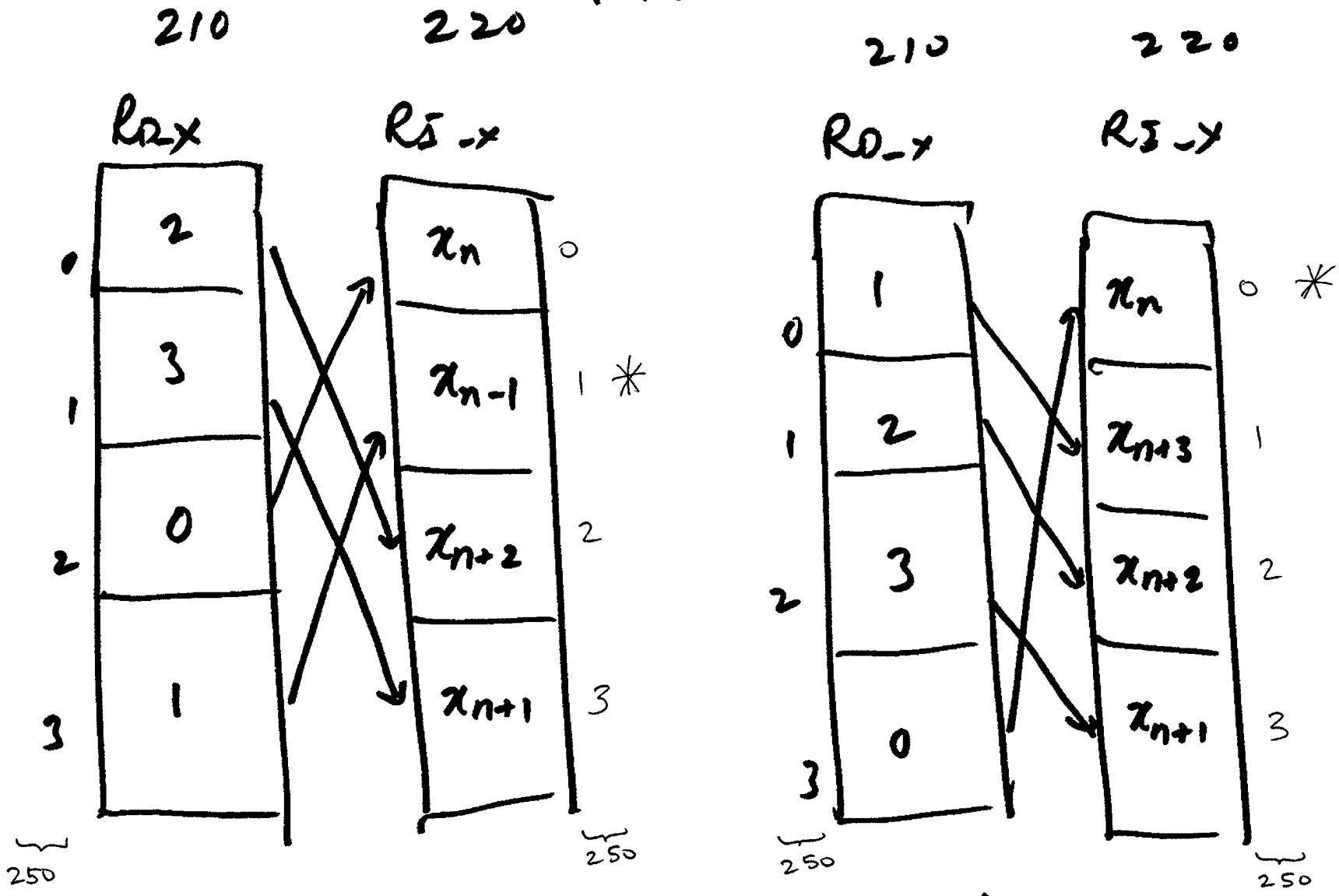

210
220
R_{2_x}
R_{3_x}
2
3
0
1
x_n
x_{n-1}
x_{n+2}
x_{n+1}
0
1 *
2
3
250
250
t: n+2
201
210
220
R_{0_y}
R_{3_y}
1
2
3
0
x_n
x_{n+3}
x_{n+2}
x_{n+1}
0 *
1
2
3
250
250
t: n+3
202

FIGURE 3

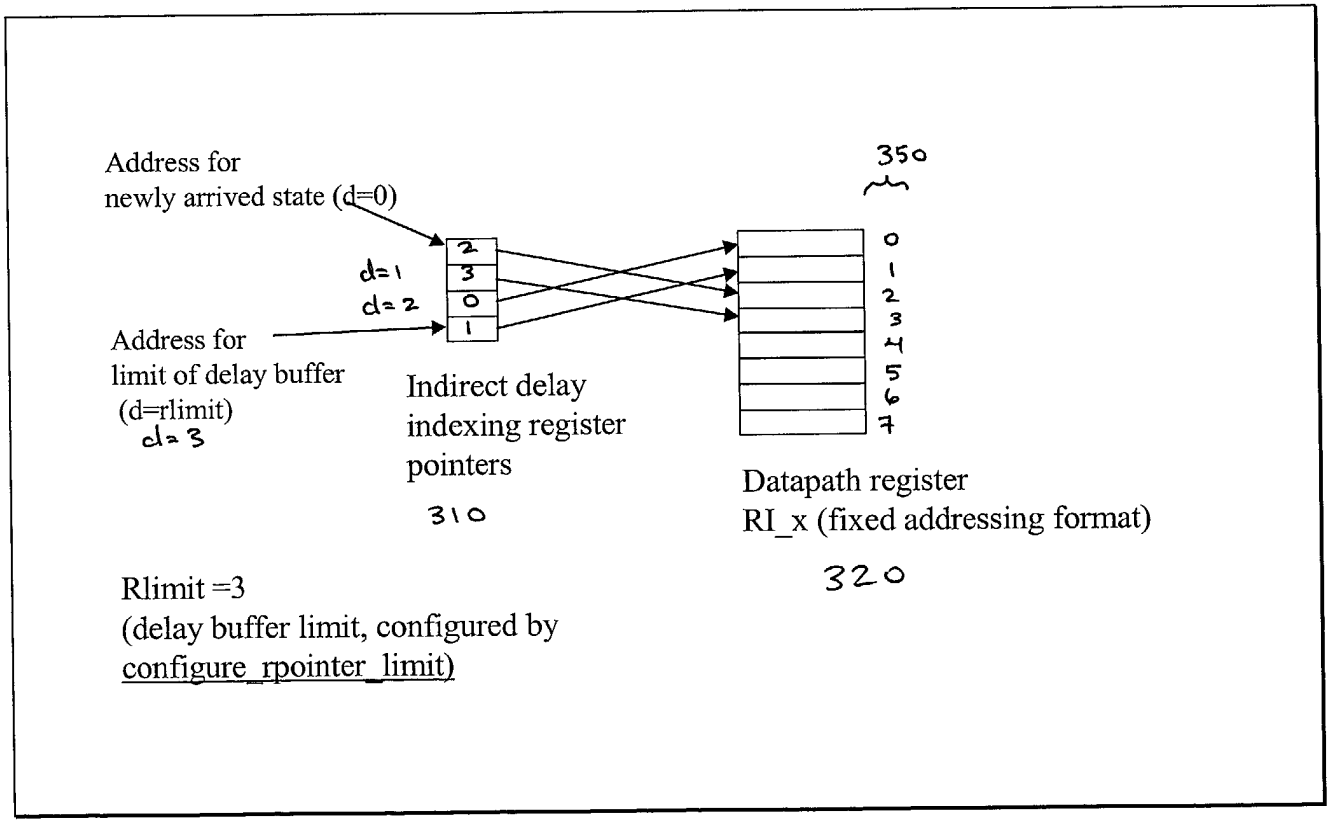
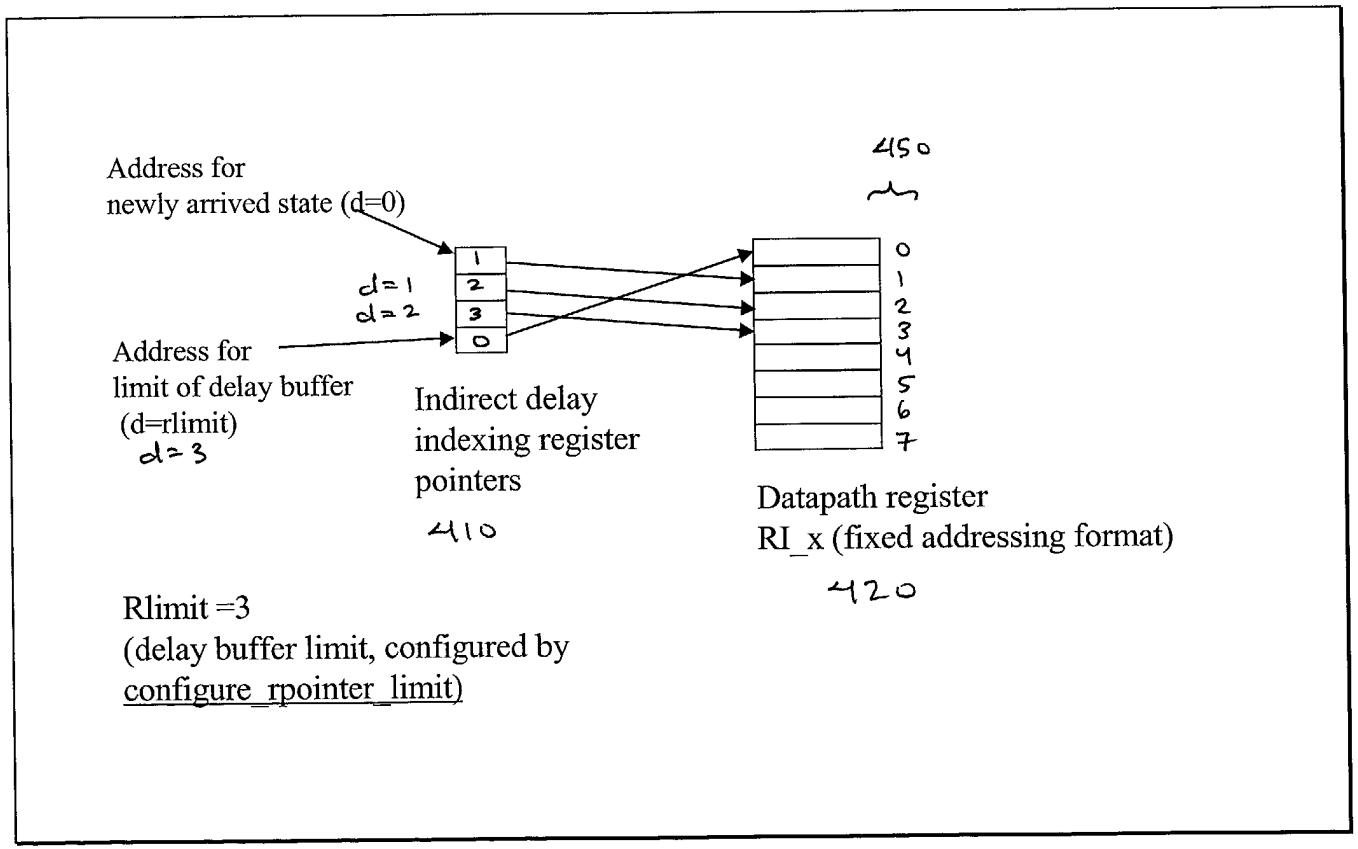
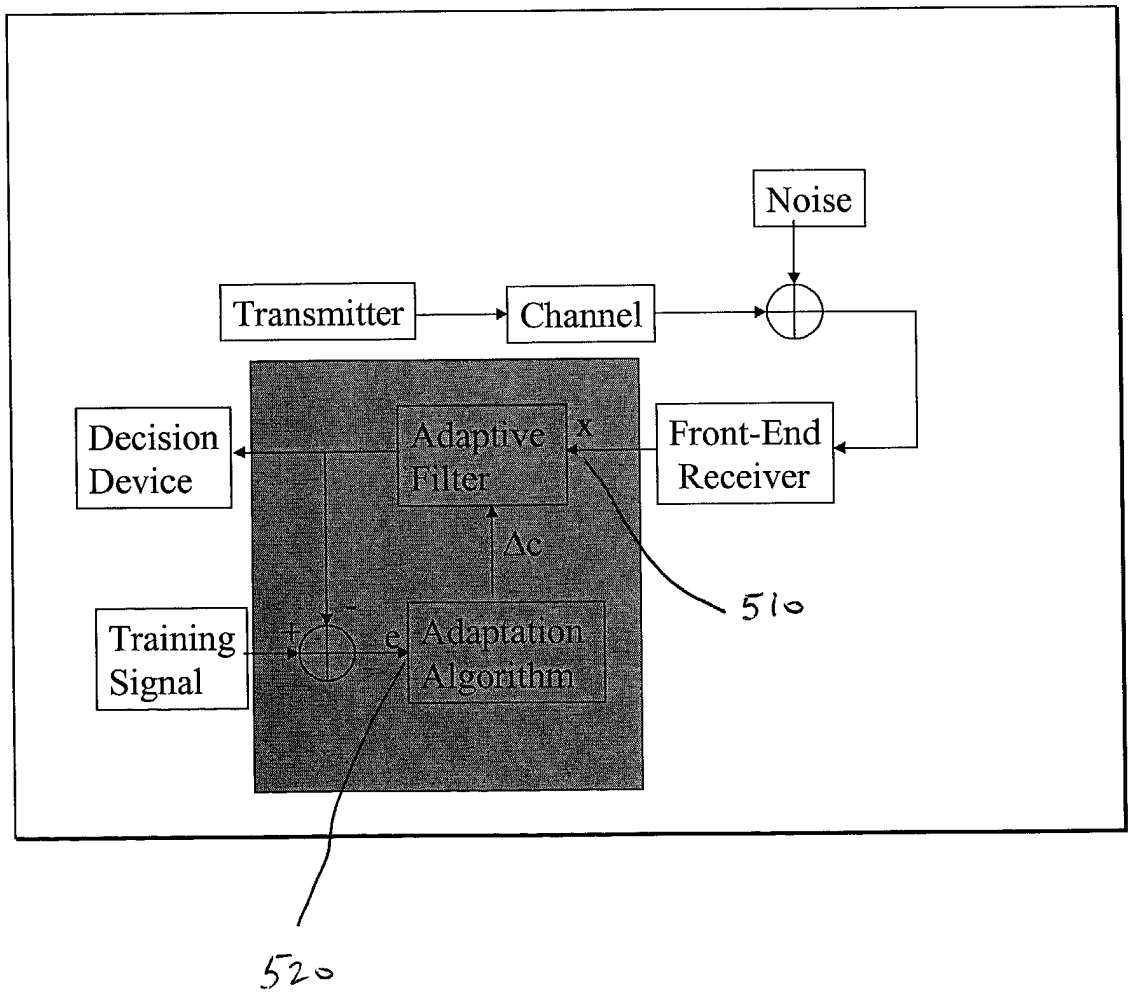

Address for
newly arrived state (d=0)
d=1
d=2
Address for
limit of delay buffer
(d=rlimit)
d=3
2
3
0
1
Indirect delay
indexing register
pointers
310
350
0
1
2
3
4
5
6
7
Datapath register
RI_x (fixed addressing format)
320
Rlimit =3
(delay buffer limit, configured by
configure_rpointer_limit)

FIGURE 4


Address for
newly arrived state (d=0)
d=1
d=2
Address for
limit of delay buffer
(d=rlimit)
d=3
1
2
3
0
Indirect delay
indexing register
pointers
410
450
0
1
2
3
4
5
6
7
Datapath register
RI_x (fixed addressing format)
420
Rlimit =3
(delay buffer limit, configured by
configure_rpointer_limit)

TARGET DESIGNS

FIGURE 5



Forcast Research

FIGURE 6

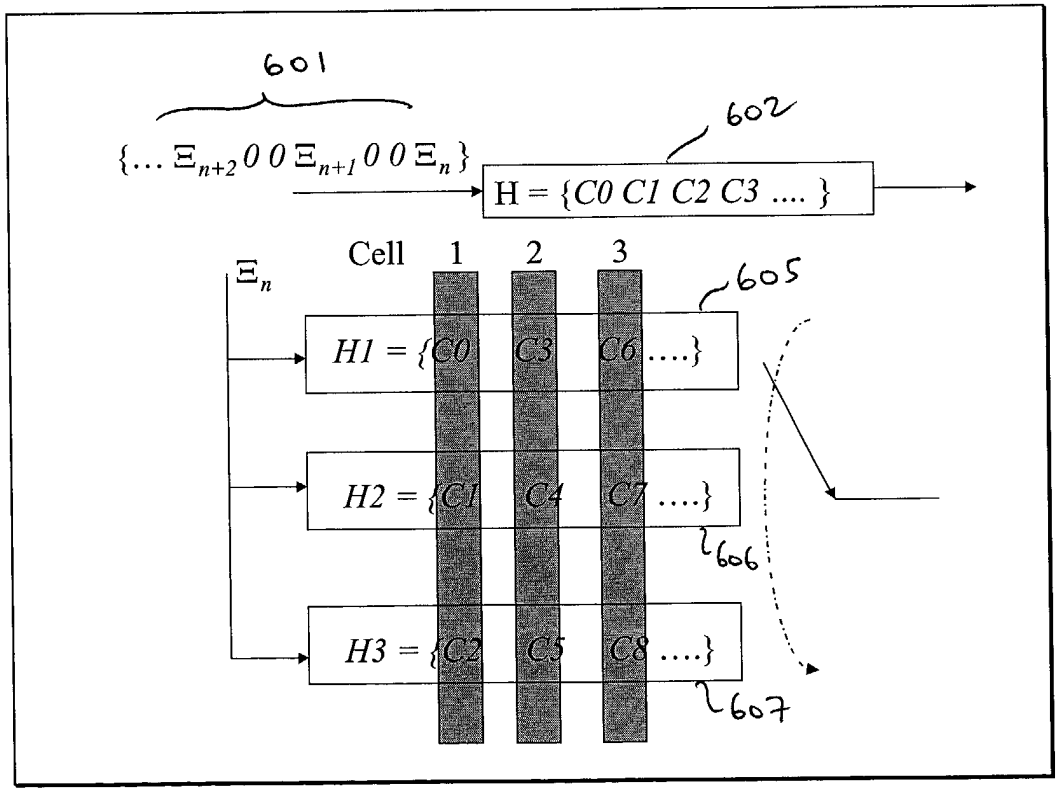


FIGURE 7

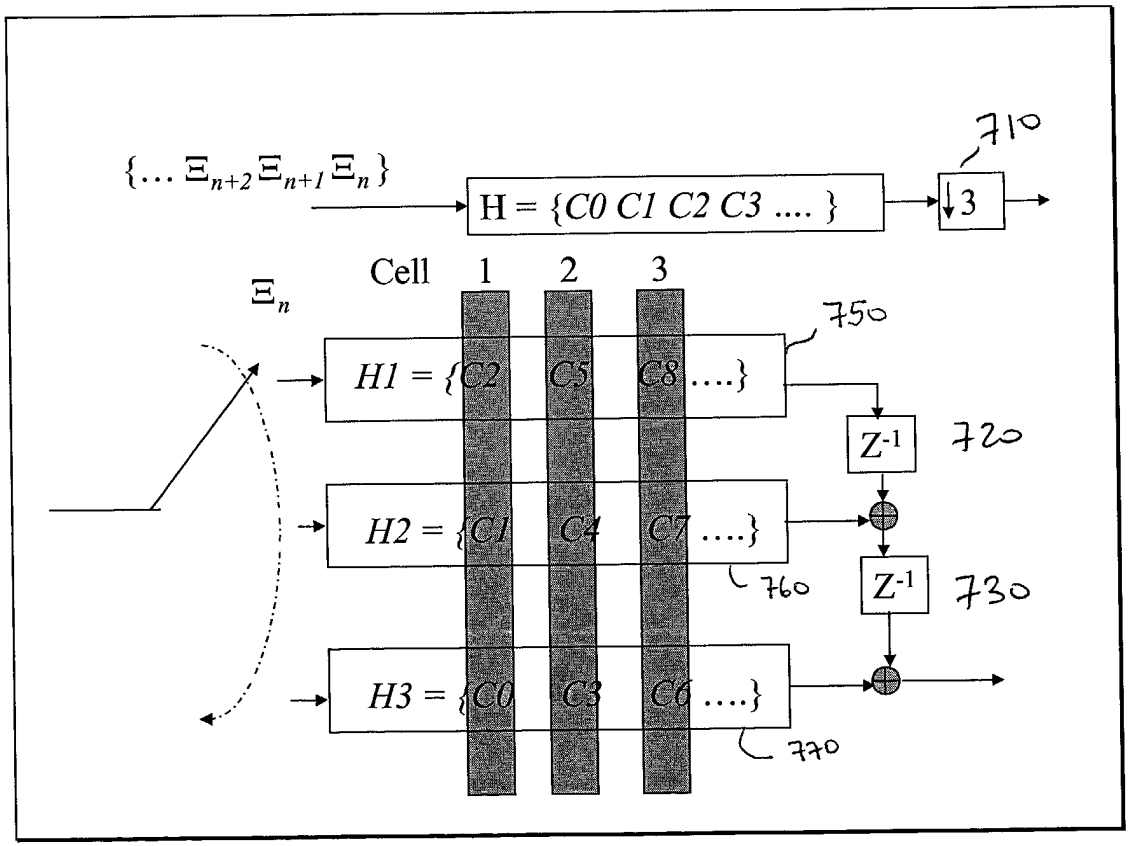
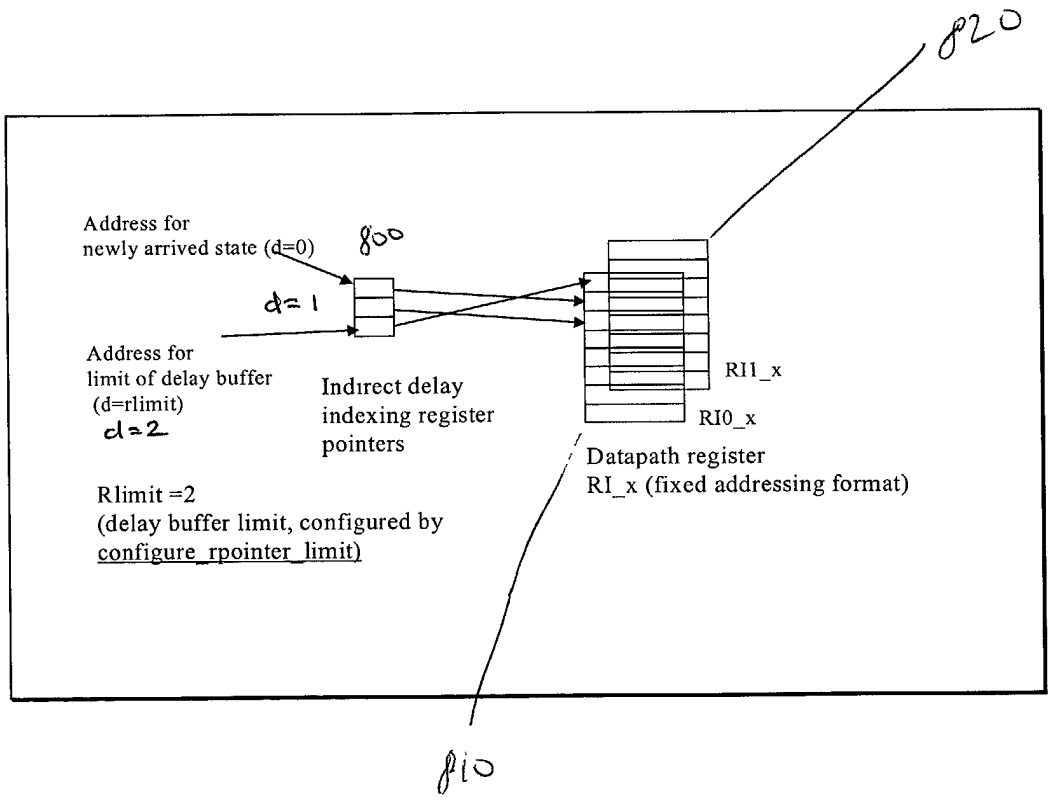

{... Ξn+2 Ξn+1 Ξn }
H = {C0 C1 C2 C3 .... }
710
3
Cell 1 2 3
Ξn
750
H1 = {C2 C5 C8 ....}
Z-1
720
H2 = {C1 C4 C7 ....}
760
Z-1
730
H3 = {C0 C3 C6 ....}
770

FIGURE 8


820
Address for
newly arrived state (d=0)
800
d=1
Address for
limit of delay buffer
(d=rlimit)
d=2
Indirect delay
indexing register
pointers
RI1_x
RI0_x
Datapath register
RI_x (fixed addressing format)
Rlimit =2
(delay buffer limit, configured by
configure_rpointer_limit)
810